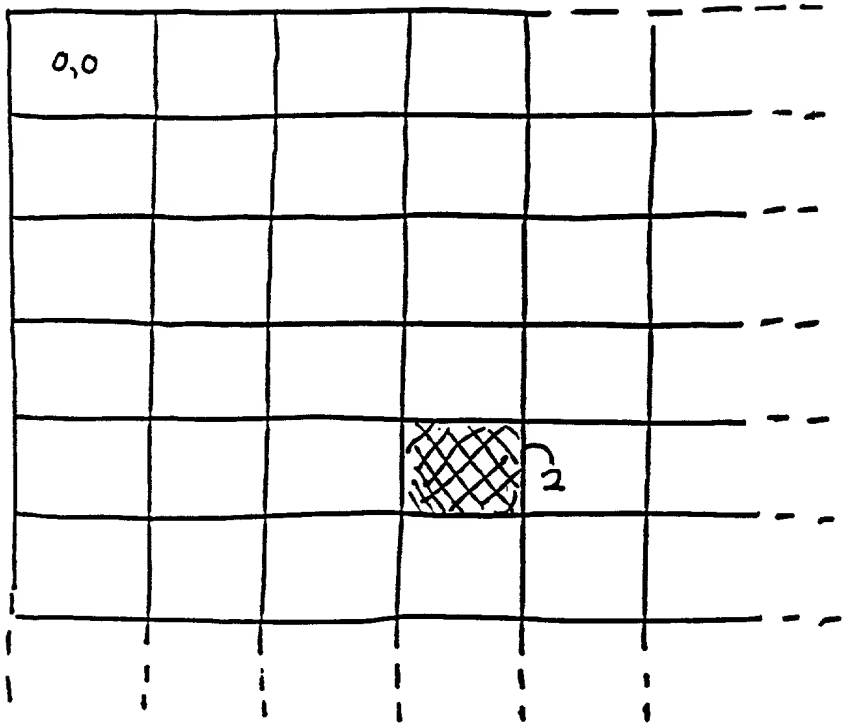
0,0
2

FIG. 1

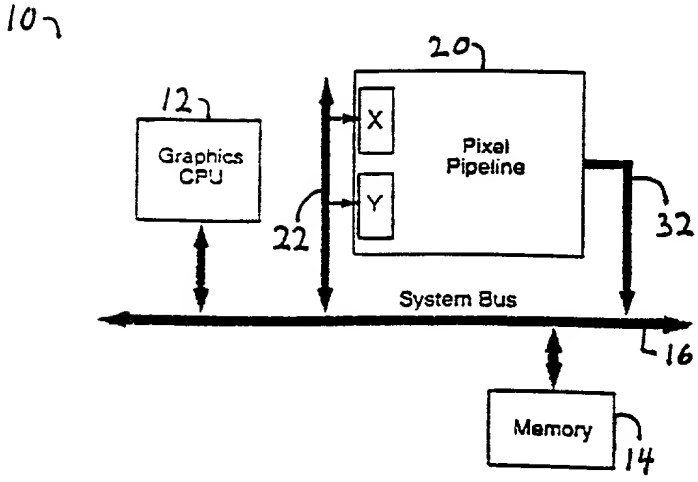
10
20
12
Graphics CPU
X
Y
Pixel Pipeline
22
32
System Bus
16
Memory
14

FIG. 2

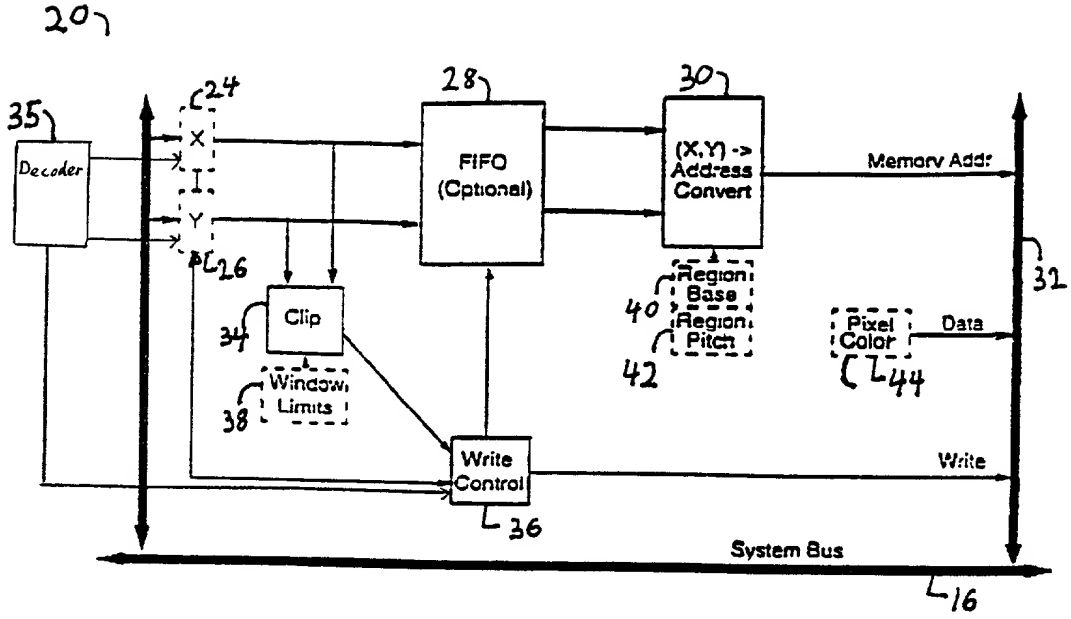
20
35
Decoder
24
X
Y
26
28
FIFO
(Optional)
30
(X,Y) ->
Address
Convert
Memory Addr
32
Region
Base
40
Region
Pitch
42
Pixel
Color
44
Data
Clip
34
Window
Limits
38
Write
Control
36
Write
System Bus
16

FIG. 3

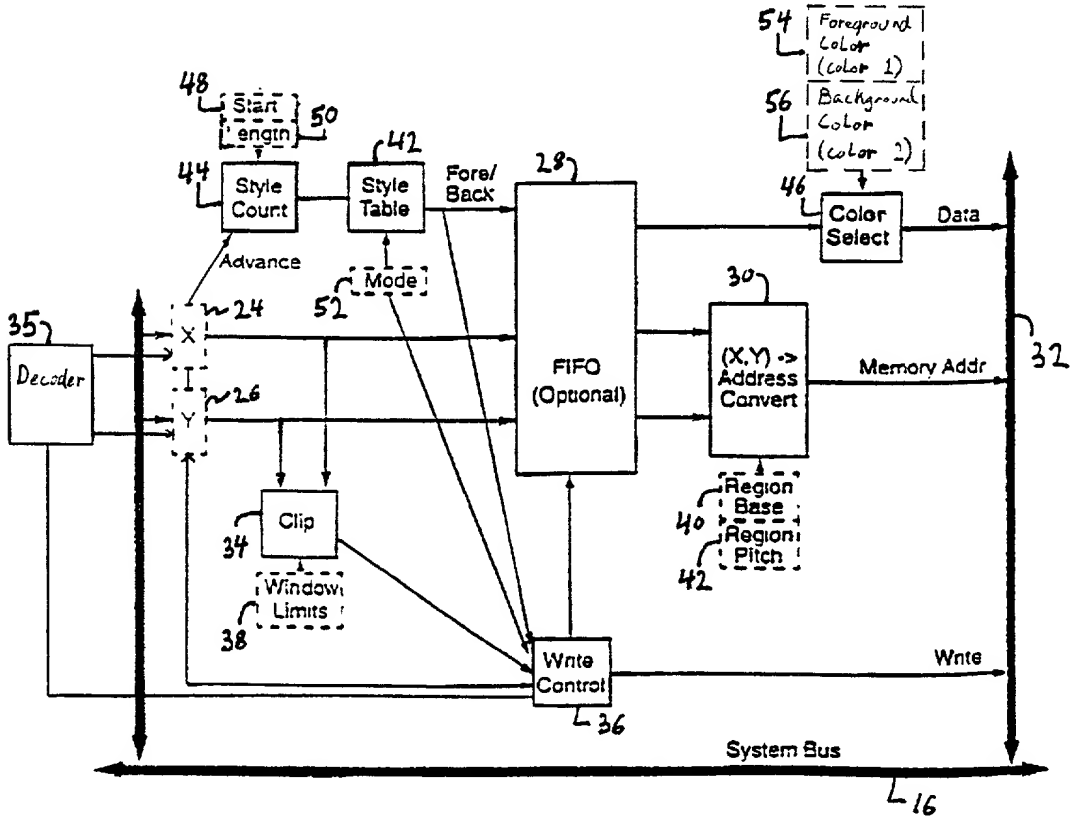
54
Foreground
Color
(color 1)
56
Background
Color
(color 2)
48
Start
Length
50
44
Style
Count
42
Style
Table
Fore/
Back
28
46
Color
Select
Data
Advance
Mode
52
30
35
Decoder
24
X
Y
26
FIFO
(Optional)
(X,Y) ->
Address
Convert
Memory Addr
32
Region
Base
40
Region
Pitch
42
Clip
34
Window
Limits
38
Write
Control
36
Write
System Bus
16

FIG. 4

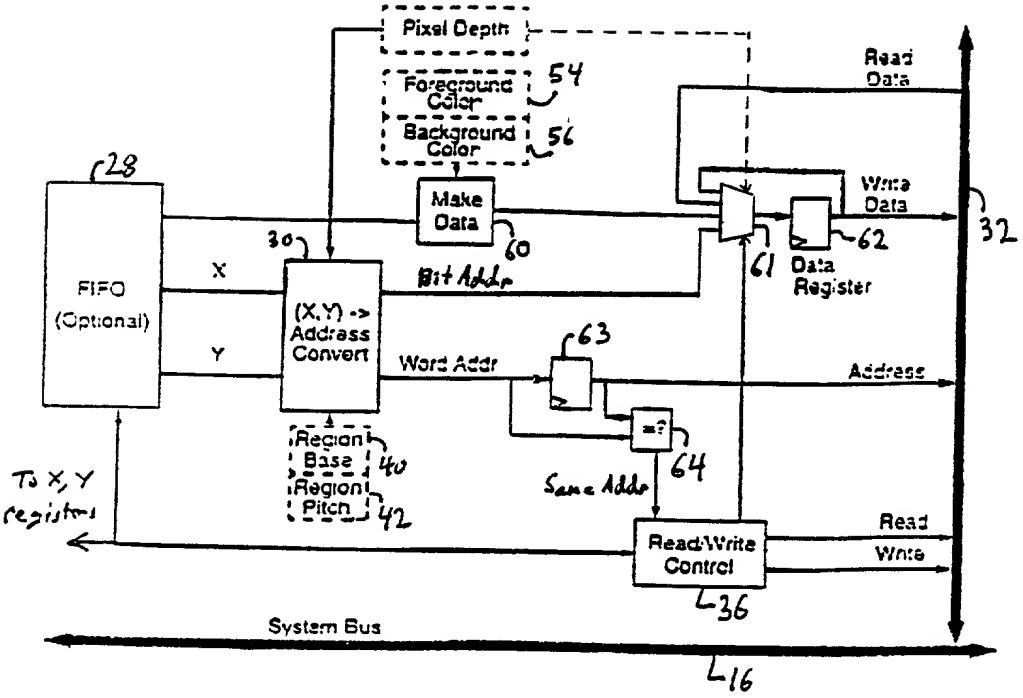
Pixel Depth
Foreground Color
54
Background Color
56
28
Make Data
60
Read Data
Write Data
32
62
61
Data Register
30
FIFO (Optional)
X
Y
(X,Y) -> Address Convert
Bit Addr
63
Word Addr
Address
=?
64
Region Base
40
Region Pitch
42
To X, Y registers
Same Addr
Read/Write Control
36
Read
Write
System Bus
16

FIG. 5